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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,769	09/23/2003	Kenneth R. Smits	42P11022C	4381

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EXAMINER	
ROJAS, MIDYS	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,769	SMITS, KENNETH R.	
	Examiner	Art Unit	
	Midys Rojas	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 10/14/2005 have been fully considered but they are not persuasive.

Applicant argues that the signal lines of Kronstadt (RAS_{1-n} and CAS_{1-n}) only carry signals to address the banks of the cache and do not carry information from the cache banks. However, Kronstadt refers to these signals lines as inputs and outputs to the controller 18; therefore, information from the cache banks must be carried to the controller (see Col. 3, lines 9-25). Additionally, these signals lines are represented with a bi-directional signal line between the memory controller and the system of Figure 3, implying that information from the cache banks is carried to the controller.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 7, 9, and 12-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kronstadt et al. (4,725,945).

Regarding Claim 1, Kronstadt teaches a memory 12 (Figure 4) comprising: a plurality of arrays of memory cells (memory banks 1- n), the arrays being arranged in banks, each bank including regular arrays (array of static column mode dynamic random access memories, Column 2, lines 11-28) and a redundant array (supports one or more redundant memory banks,

Column 4, lines 25-45); a bus having data lines to transmit information from the regular arrays and to transmit information from the redundant array (data lines RAS_{1-n} and CAS_{1-n} on Figure 4 also denoted as a single bi-directional signal line between the memory controller and the system of Figure 3); circuitry to connect (controller 18) a first set of information from the regular array to a first set of the data lines and to connect a second set of information from the regular array and the redundant array to a second set of the data lines (Figure 4, data lines RAS_{1-n} and CAS_{1-n}). Memory controller 18 controls the data lines connecting to the different memory banks (Column 3, lines 9-20). Kronstadt describes these connection lines (RAS_{1-n} and CAS_{1-n}) as data lines (signal lines, Col. 3, lines 9-25).

Regarding Claims 7 and 12, Kronstadt discloses a memory 12 (Figure 4), comprising: a plurality of arrays of memory cells, the arrays being arranged in banks (banks 1 – n), each bank including regular arrays (array of static column mode dynamic random access memories, Column 2, lines 11-28), A.sub.0-N, and a redundant array (supports one or more redundant memory banks, Column 4, lines 25-45); a data bus having sets of N+1 sets of bus lines, B.sub.0-N, to communicate data from the regular arrays and to said redundant array (Figure 4, data lines RAS_{1-n} and CAS_{1-n}); logic associated with each array (controller 18), to communicate data from an ith regular array to an ith set of the bus lines, with the redundant array being disconnected from the data bus; wherein the logic is to disconnect the regular array, A.sub.i, from the data bus and to connect the redundant array to the data bus in response to a change in state of a bit associated with a cache bank. In instances where invalid banks are identified prior to an access, the access of an invalid bank is avoided. In this system, the invalid bank can be avoided by disabling the data line to such bank. In this case, the data line is not affected, but its connection

to the invalid bank may be discontinued (Column 3, lines 15-45 and Column 4, lines 6-14). This is demonstrated by the instance in which banks are labeled invalid and a cache miss occurs until the banks are labeled valid again. The system avoids access to invalid banks. Kronstadt describes these connection lines (RAS_{1-n} and CAS_{1-n}) as data lines (signal lines, Col. 3, lines 9-25).

Regarding Claims 2 and 13, Kronstadt discloses the memory of claim 1 wherein the circuitry (controller 18) comprises a bit (valid field) that, when set to a first logic state (identifies invalid banks), causes the circuitry to disconnect the regular array from the bus. In instances where invalid banks are identified prior to an access, the access of an invalid bank is avoided if possible. In this system, the invalid bank can be avoided by disabling the data line to such bank. In this case, the data line is not affected, but its connection to the invalid bank may be discontinued (Column 3, lines 15-45).

Regarding Claim 3, if the redundant bank is identified as a valid bank, such identification ("setting of the bit") can cause the controller to connect the redundant banks to a data line (See Figure 4).

Regarding Claims 4-5 and 9, the banks of Kronstadt et al. are arranged in a vertical linear configuration (See Figure 4) in which each banks is placed in one of multiple rows.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 10 and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Kronstadt et al. (4,725,945) in view of Parulkar (6,769,081).

Regarding Claims 10 and 14, Kronstadt teaches the invention of Claims 7 and 12 above. The controller of Kronstadt et al. has circuitry to set a bit in accordance to the validity of a bank. However, Kronstadt does not teach setting the conductivity of a fuse to change the status of a bit. Parulkar discloses a programmable fuse used to set an address bit (Column 4, lines 30-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to set the bit of Kronstadt in the same manner as that of Parulkar because fuses are commonly found as components in computer systems and setting a fuse's conductivity is a quick and effective way to affect that value of a bit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 27th, 2005

Midys Rojas
Examiner
Art Unit 2185

MR

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER